What Is Claimed Is:

1. Multi-functional digital signal processing circuitry comprising:

first, second, and third multiplier circuitries;

first, second, and third input adder circuitries for selectively producing sums of inputs for use by the multiplier circuitries; and

first, second, and third output adder circuitries for selectively combining outputs of the multiplier circuitries.

2. The circuitry defined in claim 1 further comprising:

a plurality of registers for storing at least some of the inputs.

3. The circuitry defined in claim 2 further comprising:

interconnection circuitry for allowing contents of selected ones of the registers to be selectively shifted to selected others of the registers.

4. The circuitry defined in claim 1 further comprising:

circuitry for selectively nulling an input to at least one of the input adder circuitries.

5. The circuitry defined in claim 1 further comprising:

selection circuitry for deriving an input to at least one of the multiplier circuitries

from a source other than one of the input adder circuitries.

6. The circuitry defined in claim 1 wherein at least one of the output adder circuitries is configured to subtract.

7. The circuitry defined in claim 1 wherein at least one of the output adder circuitries is controllable to add or subtract.

8. The circuitry defined in claim 1 wherein at least one of the input adder circuitries is controllable to either separately add plural pairs of relatively short inputs or one pair of relatively long inputs.

9. The circuitry defined in claim 1 wherein at least one of the multiplier circuitries is controllable to either separately perform plural relatively short multiplications or one relatively long multiplication.

10. The circuitry defined in claim 1 wherein at least one of the output adder circuitries is controllable to either separately add plural pairs of relatively short inputs or one pair of relatively long inputs.

11. The circuitry defined in claim 2 further comprising:

interconnection circuitry for allowing successive data samples to be shifted through the registers so that each sample is present in the

register for as long as it is needed as an input to a finite impulse response filter function.

12. The circuitry defined in claim 11 further comprising:

connections for applying the contents of a pair of registers to at least one of the input adder circuitries, the registers in the pair containing two samples to which a common multiplier is applied in the finite impulse response filter function.

13. The circuitry defined in claim 11 wherein the interconnection circuitry is controllable to selectively skip at least one of the registers through which the samples are shifted depending on whether the finite impulse response filter function is of odd or even order.

14. The circuitry defined in claim 1 wherein the inputs comprise real and imaginary parts of two complex numbers to be multiplied, and wherein the circuitry further comprises:

input connections for applying the real parts to the first multiplier circuitry, for applying the imaginary parts to the second multiplier circuitry, and for applying the real and imaginary parts to the third input adder circuitry to produce sums for use by the third multiplier circuitry.

15. The circuitry defined in claim 1 wherein the first and second output adder circuitries are connected to selectively combine outputs of the first and second multiplier circuitry.

16. The circuitry defined in claim 15 wherein the third output adder circuitry is connected to selectively combine outputs of the second output adder circuitry and the third multiplier circuitry.

17. A programmable logic device including circuitry as defined in claim 1.

18. The programmable logic device defined in claim 17 further comprising:

routing circuitry for selectively supplying signals to and receiving signals from the multi-functional digital signal processing circuitry.

19. The programmable logic device defined in claim 18 further comprising:

programmable logic circuitry connected to the routing circuitry.

20. A digital processing system comprising:

processing circuitry;

a memory coupled to the processing circuitry; and

a programmable logic device as defined in claim 17 coupled to the processing circuitry and the memory.

21. A printed circuit board on which is mounted a programmable logic device as defined in claim 17.

22. The printed circuit board defined in claim 21 further comprising:

a memory mounted on the printed circuit board and coupled to the programmable logic device.

23. The printed circuit board defined in claim 21 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the programmable logic device.

24. DSP circuitry comprising:

a plurality of registers;

circuitry for selectively shifting data among the registers;

a plurality of input adder circuits for selectively operating on selected signals from the registers;

a plurality of multiplier circuits for selectively operating on selected signals from the input adder circuits; and

a plurality of output adder circuits for selectively operating on selected signals from the multiplier circuits.

25. The circuitry defined in claim 24 further comprising:

circuitry for alternatively selecting some of the signals for at least one of the multiplier circuits to operate on from a source other than the input registers.

26. The circuitry defined in claim 24 wherein at least one of the input adder circuits is selectively able to operate either as two, separate, relatively small adder circuits or as one relatively large adder circuit.

27. The circuitry defined in claim 24 wherein at least one of the multiplier circuits is

selectively able to operate either as two, separate, relatively small multiplier circuits or as one relatively large multiplier circuit.

28. The circuitry defined in claim 24 wherein at least one of the output adder circuits is selectively able to operate either as two, separate, relatively small adder circuits or as one relatively large adder circuit.

29. The circuitry defined in claim 24 wherein at least one of the output adder circuits is selectively able to subtract.

30. The circuitry defined in claim 24 wherein the plurality of multiplier circuits consists of three multiplier circuits.

31. DSP circuitry comprising:

a plurality of registers;

a plurality of multiplier circuits;

at least one input adder circuit associated with each of the multiplier circuits for selectively adding outputs of selected ones of the registers to provide a first set of inputs to the associated multiplier circuit; and

at least one input selection circuit associated with each of the multiplier circuits for selecting from (a) outputs of selected ones of the registers and (b) signals external to the DSP circuitry to provide a second set of inputs to the associated multiplier circuit.

32. The DSP circuitry defined in claim 31 further comprising:

register input selection circuitry associated with each of the registers for selecting from (a) outputs of another one of the registers and (b) signals external to the DSP circuitry to provide inputs to the associated register.

33. The DSP circuitry defined in claim 31 wherein at least one of the multiplier circuits has associated additional input adder circuitry and associated additional input selection circuitry, the additional input adder circuitry adding outputs of selected one of the registers different than the register outputs addable by the input adder circuit associated with that multiplier circuit, and the additional input selection circuitry being operable to selectively provide the first set of inputs to that multiplier circuit from the additional input adder circuitry.

34. The DSP circuitry defined in claim 33 wherein the at least one of the multiplier circuits has associated further input adder circuitry for adding outputs of selected ones of the registers different than the register outputs addable by the input adder circuit and the additionally input adder circuitry associated with that multiplier circuit, and wherein the input selection circuit associated with that multiplier is additionally able to select outputs of the further input adder circuitry as the second set of inputs to that multiplier circuit.

35. The DSP circuitry defined in claim 31 wherein each of the multiplier circuits separately multiplies (a) first portions of the first and second

sets of inputs to that multiplier circuit and (b) second portions of the first and second sets of inputs to that multiplier circuit to produce first and second products.

36. The DSP circuitry defined in claim 35 wherein each of the multiplier circuits can separately output the first and second products.

37. The DSP circuitry defined in claim 36 wherein each of the multiplier circuits can alternatively combine the first and second products as partial products to produce a third product.

38. The DSP circuitry defined in claim 31 further comprising:

an output adder circuit associated with each of the multiplier circuits, each of the output adder circuits being connected to add outputs of the associated multiplier circuit and outputs of another circuit selected from the group consisting of another multiplier circuit and another output adder circuit.